

WHAT IS CLAIMED IS:

1. An insulated gate bipolar transistor comprising:

5 a semiconductor substrate of a first conductivity type including a first main surface and a second main surface;

an insulated gate transistor formed in a region of said semiconductor substrate on a side of said semiconductor substrate where said first main surface is included, said insulated gate transistor including a channel of said first conductivity type which is formed within a base region of a second conductivity type during an on state of said
10 insulated gate transistor, said base region extending from said first main surface toward an interior of said semiconductor substrate;

a first main electrode formed on said first main surface and being in contact with said base region of said insulated gate transistor at said first main surface;

15 a first semiconductor layer of said first conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor;

a second semiconductor layer of said second conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; and

20 a second main electrode formed on said first semiconductor layer and said second semiconductor layer,

wherein an interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer is parallel to said first main surface,

25 a distance between said first main surface and said interface is equal to $200\text{ }\mu\text{m}$ or smaller, and

a thickness of each of said first semiconductor layer and said second semiconductor layer is equal to $2\text{ }\mu\text{ m}$ or smaller.

2. The insulated gate bipolar transistor according to claim 1,
5 wherein a first interface between said first semiconductor layer and said second main electrode occupies 20-70% of said interface.

3. The insulated gate bipolar transistor according to claim 1,
wherein a second interface between said second semiconductor layer and said
10 second main electrode occupies 30-80% of said interface.

4. The insulated gate bipolar transistor according to claim 1,
wherein a total width of a first width of said first semiconductor layer and a
second width of said second semiconductor layer which are parallel to said first main
15 surface and extend along a direction in which said first semiconductor layer and said second semiconductor layer are aligned is in a range from $50\text{ }\mu\text{ m}$ to $200\text{ }\mu\text{ m}$.

5. The insulated gate bipolar transistor according to claim 1,
wherein said semiconductor substrate includes an additional semiconductor
20 layer of said first conductivity type which extends from an interface between said base region and said semiconductor substrate toward said interior of said semiconductor substrate, and
an impurity concentration of said additional semiconductor layer is higher than
that of a portion of said semiconductor substrate which forms an interface with said
25 additional semiconductor layer.

6. An inverter circuit comprising:

the insulated gate bipolar transistor according to claim 1,

wherein said insulated gate bipolar transistor functions as a switching device

5 with a built-in freewheeling diode.

7. A method of manufacturing an insulated gate bipolar transistor, comprising the steps of:

forming an MOSFET cell in a region of a semiconductor substrate of a first
10 conductivity type on a side of said semiconductor substrate where a first main surface thereof is included;

forming a first semiconductor layer of said first conductivity type and a second
semiconductor layer of a second conductivity type adjacent to said first semiconductor
layer such that each of said first and second semiconductor layers extends from a portion
15 of a second main surface of said semiconductor substrate which faces said MOSFET cell toward an interior of said semiconductor substrate, after forming said MOSFET cell; and

forming a second main electrode in contact with said first and second
semiconductor layers on said second main surface comprising said first and second
semiconductor layers formed thereon.

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8. The method of manufacturing an insulated gate bipolar transistor according to claim 7,

wherein a first main electrode and said second main electrode are formed on
said first main surface and on said second main surface of said semiconductor substrate,
25 respectively, after forming said first and second semiconductor layers.

9. The method of manufacturing an insulated gate bipolar transistor according to claim 7, further comprising the step of:

5 polishing said semiconductor substrate from said second main surface to make a thickness of said semiconductor substrate equal to $200\text{ }\mu\text{ m}$ or smaller after forming said MOSFET cell and before forming said first and second semiconductor layers.

10. The method of manufacturing an insulated gate bipolar transistor according to claim 9, further comprising:

10 forming a projection serving as a mask alignment mark in a region of said semiconductor substrate on a side of said semiconductor substrate where said second main surface is included, after polishing said semiconductor substrate and before forming said first and second semiconductor layers.

15 11. The insulated gate bipolar transistor according to claim 5, wherein said insulated gate transistor includes a trench MOSFET cell.